ACBEL POLYTECH INC.

R1C Series 550W

-48VDC Power Module Specification

Model Number: R1CD2551A Series
AcBel PN: FSE039-00AG

Note: Outward Airflow

Revision: A07
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Released by: MF Chen
Change Date: 2019/07/10
Changed by: Leo Wang

REVISION LOG

DATE	SECTION	REVISION	ISSUE / DESCRIPTION
2015/05/21		S00	Original release
2016/01/02		S01	Modify SPEC EMC、Surge
2016/05/16	2.1.2	S02	Modify Input Current
	2.1.6		Modify Surge Immunity description
	2.2		Modify Brownout -38VDC→-34VDC
	4.1		Modify PSON# Signal Characteristic
	4.2		Modify PWOK/PG delay time
	4.5		Add share bus define
	4.5.1		Add current share define
	4.7		Add remote sense define
	5.3		Delete over temperature protection timeing for SMBAlert
	7		Add cold redundant define
	8.3		Modify sensor accuracy table
	9.6		Add EMI/EMC requirements
	10.3		Modify Hi-pot test condition
	13		Update mechanical drawing
	13.1		Update DC input connector type
2016/05/24	4.5.1		Modify current share define
2016/05/30	5.3		Modify OVER TEMPERATURE PROTECTION
2016/08/10	4.5	S03	Change Ishare slope requirement from 5V to 8V so AC and DC can current share.
	4.5.1		Add Hot Swap requirement
	5.3		Add UVP
	5.4		Input Fail
	5.5		OTP based on sensor reading
	5.6		FAN CTRL Algorythmn
	8.2.1		Add FRU requirement.
2016/08/17	2.3.2	A00	Change wording of SMBAlert recover and Table expression for better understanding.
	4.3		Remove Power, only Temp, Input and OCW
2016/09/05	4.4	S05	CR_BUS low time change from 100uS to 300uS
	2.3.2		Change “≥” to “>” for OCP1, OCP & OPP
	4.3		Change Input Failure warning to Input UV failure
	8.1.2		Change i2c noise requirement to 600mV (TBD).

	8.3		Change Temp Accuracy from ±3°C to ±5°C o(TBD)
	5.4		Change Input range from -32 ~ 76VDC to -36 ~ -72VDC
	5.3		Change Output UV from 10.8V to 10.0V
			Change from AC to Input
2016/09/06	10.1	A00	Product Safety Compliance Delete BSMI
2016/10/13	3.	A01	Timing requirements for Main add: Tvout_on & Tvout_off does not apply for single (Main) output power supplies.
	8.3		Change Accuracy to introduce min. fixed fault.
	4.4		CR_BUS rise and fall time change from 300uS to 100uS
	7.1		CR_BUS will immediately turn on within 300uSec
2016/10/19	5.5	A02	$T_{Pri.\ Hot\ Spot}$ Warning in °C change from 80 °C to 110 °C, Critical in °C change from 90 °C to 115 °C
2016/11/01	9.6	A03	Add GR-1089-CORE define
2016/12/20	14.	A04	Add PMBus Command List
	15.		Add IPMI FRU information
	2.3.2		Voltage Regulation change from 12V to 12.2V
	8.1.2		Change i2c noise requirement to 300mV.
2016/12/23	4.8	A05	Add Address Pin description
2017/01/09	13		Update mechanical drawing
2017/03/14	8.3	A06	Change Input current Accuracy from ±0.2A to ±0.5A ; Input power Accuracy from ±5W to ±10W
2019/07/10	2.1.4	A07	Modify power recover description
	5.5		Modify over temperature protection table

1. GENERAL SCOPE

This specification describes the performance characteristic of an **550W** hot swappable -48V DC-DC switching power supply module with a +12V main DC output and a +12Vsb auxiliary output. The power supply shall be able to operate as a single supply or in an N+1 parallel hot-plug able operation with active load sharing in an N+1 redundant configuration.

2. ELETRICAL PERFORMANCE

This Chapter describes the electrical requirements and performance compliances of ***R1CD2551A*** power supply.

2.1 POWER INPUT SPECIFICATION

2.1.1 DC Input Voltage

PARAMETER	MIN	Normal	MAX
Voltage	-36Vdc	-48Vdc	-72Vdc

2.1.2 Inrush Current/ Input Current

Input current shall meet the limits shown in the following table:

Input Voltage	Maximum Continuous Input current	Inrush Current	Inrush Current
-36 VDC	20A	100 A for 2usec	30 A for 5ms
-48 VDC	14A	100 A for 2usec	30 A for 5ms
-72 VDC	9A	100 A for 2usec	30 A for 5ms

2.1.3 Efficiency

For the nominal input voltage (-48V), the efficiency shall be 85% or better at 100% power output. The efficiency should measure without fan.

2.1.4 Power Recovery

The power supply shall recover automatically (auto recover) after an Input power failure. Input power failure is defined to be any loss of Input power that exceeds the dropout criteria.

if Input line drop t≤8mS@550W; t≤9mS@400W that the PSU can keep working, but PSU can auto recover in other condition.

2.1.5 Input Line Leakage Current

The maximum leakage current to ground for power supply system shall not exceed 3.5mA when tested at -75Vdc Input voltages.

2.1.6 Surge Immunity

The power supply shall be tested with the system for immunity to DC input Unidirectional wave; 1kV common mode(-48V to FG or RTN to FG) and 500V differential mode(-48V to RTN), per EN 55024: 1998/A1: 2001/A2: 2003, EN 6100-4-5: Edition 1.1: 2001-04.

The pass criteria include: No unsafe operation is allowed under any condition all power supply output voltage levels to stay within proper spec levels; No change in operating state or loss of data during and after the test profile No component damage under any condition.

2.2 BROWNOUT

Below -34VDC +/- 2V the power supply shall be powered off with a minimum 2V hysteresis between the startup and shutdown voltages.

2.3 POWER OUTPUT SPECIFICATION

2.3.1 Output Power/Currents

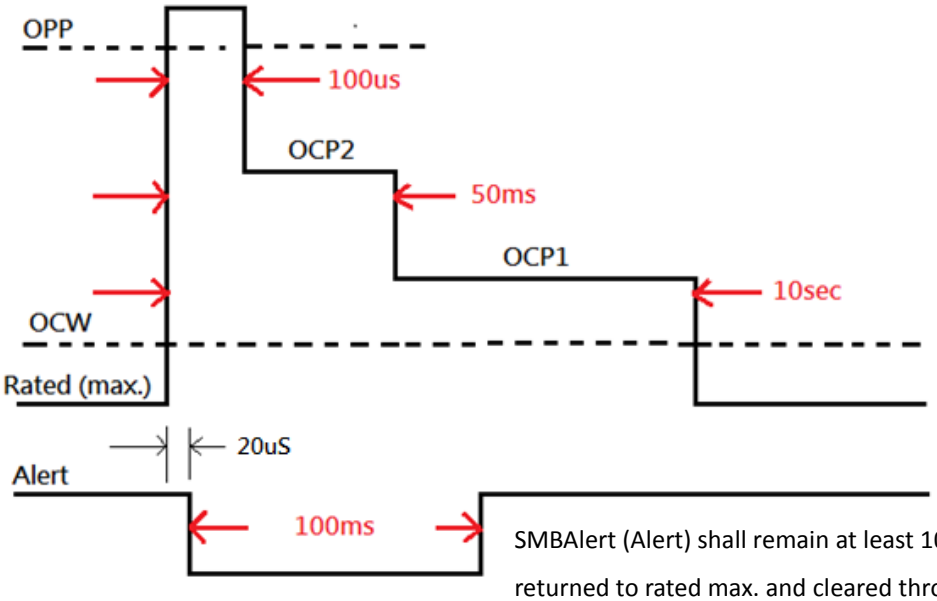
The following table defines the power and current rating of the **550W** power supply.

Voltage	Mini	Max	Peak
+12V	0.5A	45A	58.5A
+12Vsb	0.1A	3A	3.9A

1. Maximum continuous total DC output power should not exceed 550W.
2. Maximum peak total DC output power should not exceed 714W.

2.3.2 Peak Power Condition

The power supply shall meet the following peak power conditions.



SMBAlert (Alert) shall remain at least 100ms low, even if the current returned to rated max. and cleared through CLEAR_FAULTS (03h).

MIN	Parameter	MAX	Main Output Condition
> 140%	OPP	≤ 150%	Keep 100uS at least
> 125%	OCP2	≤ 140%	Keep 50mS at least
> 115%	OCP1	≤ 125%	Keep 10Sec at least
≥ 105%	OCW	≤ 115%	Continue
0%		≤ 100%	Continue

1. Peak power condition shall be following the peak power table as specify from the above. After exceeding the max. peak power threshold of T_{OFF_PEAK}, the power supply will shut down in a OPP state, and according warning and failures will be reported.
2. The warning signal (OCW) will send to system during 105% - 115% of maximum load, and shuts down after follow by the specified condition.

2.3.3 Voltage Regulation

The power supply shall stay within the following voltage limits when operating at steady state and dynamic loading conditions. These limits include the peak-peak ripple/noise conditions specified in paragraph 2.3.5. All outputs are measured with reference to the return remote sense (ReturnS) signal.

Parameter	MIN	NOM	MAX	Units	Tolerance
+12V	+11.59	+12.20	+12.81	V_{rms}	+/-5%
+12Vsb	+11.4	+12.0	+12.6	V_{rms}	+/-5%

2.3.4 Dynamic Loading

The power supply shall operate within specified limits and meet regulation requirements for step loading and capacitive loading specified below.
The load transient repetition rate shall be tested between 50Hz to 5kHz at duty cycles ranging from 10%-90%. The load transient repetition rate is only a test specification. The Δ step load may occur anywhere within the MIN load and the MAX load.

Output	△Step Load Size	Load Slew Rate	Capacitive Load
+12V	65% of max load	0.5 A/μs	2200 μF
+12Vsb	1A	0.5 A/μs	20 μF

2.3.5 Capacitive Loading

The power supply shall meet all requirements with the following capacitive loading ranges.

Output	MIN	MAX	Units
+12V	500	25,000	μF
+12Vsb	1	3100	μF

2.3.6 Ripple and Noise

Ripple and Noise shall be measured over a Bandwidth of 20MHz at the power supply output connector, with minimum capacitive load as specified within paragraph 2.2.4 in parallel with a 10μF tantalum capacitor (minimum 100mΩESR) and with a 0.1μF ceramic capacitor placed at the point of measurement. Maximum allowed ripple/noise output of the power supply is defined in table below.

+12V	+12Vsb
120 mVp-p	120 mVp-p

3. TIMING REQUIREMENTS

These are the timing requirements for the power supply operation. The output voltages must rise from 10% to within regulation limits (Tvout_rise) within 1 to 50ms, same as 12Vsb. All main outputs shall rise positive monotonically and have a slop value between 0 V/mS to 0.1V/mS.

For 12Vsb output any 5ms segment of the 10% to 90% rise time waveform, a straight line draw between the end points of the waveform segment must have s slope ≥ [Vout, nominal /20]V/mS.

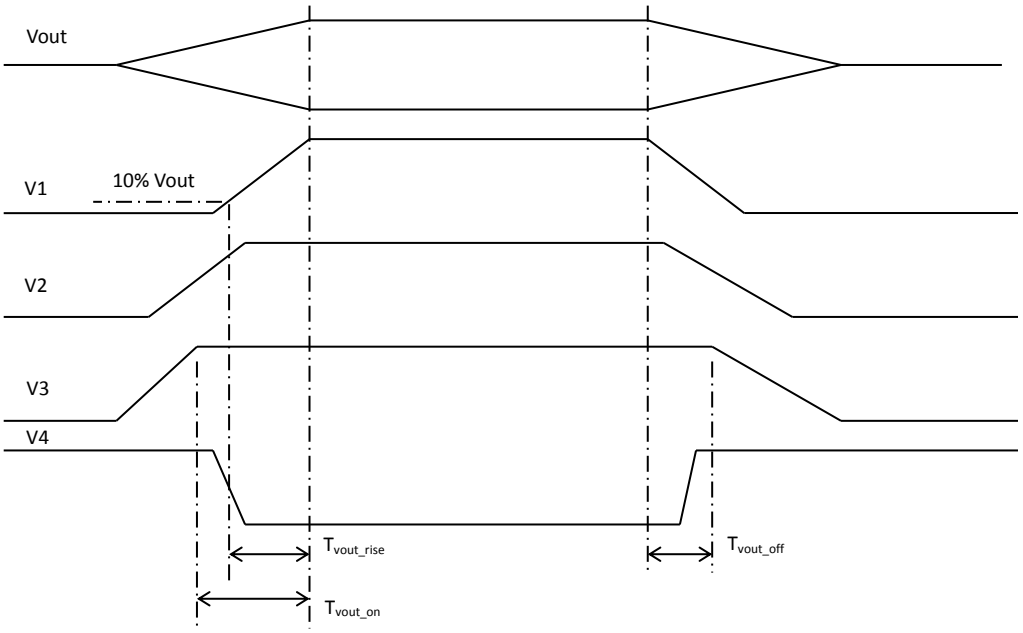
Each Main outputs voltage shall reach regulation within 50mS (Tvout_on) of each other during turn on of the power supply system. Each Main output voltage shall fall out of regulation within 400mS (Tvout_off) of each other during turn off.

Above criteria does not apply to single (Main) output power supplies.

Table below shows the timing requirements for the power supply being turned on and off via the input power, with PSON held low and the PSON signal, with the input power applied.

Item	Description	MIN	MAX	Units
$T_{vout\ rise}$	Output voltage rise time for 12V main output	1	50	ms
	Output voltage rise time for 12Vsb output	1	50	ms
T_{vout_on}	Main outputs must be within regulation of each other within this time.		50	ms
T_{vout_off}	Main outputs must leave regulation within this time.		400	ms

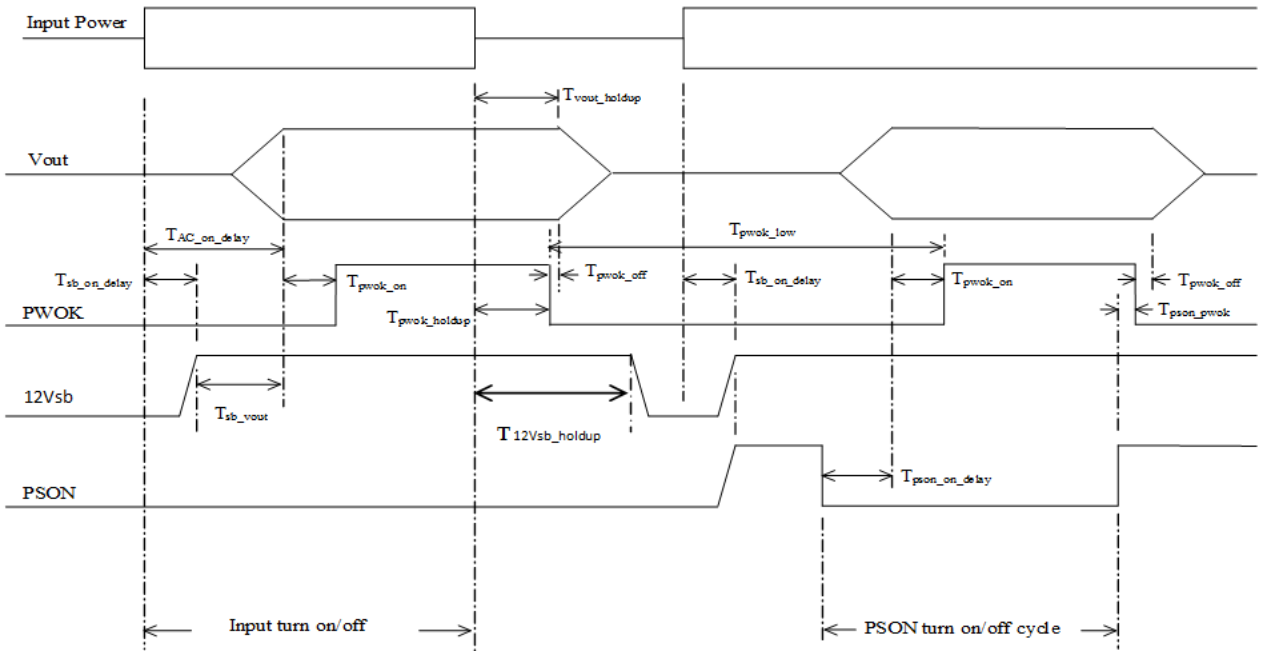
Output Voltage Timing



Turn On/Off Timing

Item	Description	MIN	MAX	UNITS
T sb_on_delay	Delay from DC input begin applied to 12Vsb begin within regulation.		1500	ms
T dc_on_delay	Delay from DC input begin applied to all output voltage begin within regulation.		3000	ms
T out_holdup	Time all output voltages stay within regulation after loss of DC input.	10		ms
T pson_on_delay	Delay from PSON# active to output voltages within regulation limits.	5	400	ms
T pson_pwok	Delay from PSON# de-active to PWOK begins de-asserted.		50	ms
T pwok_on	Delay from output voltages within regulation limits to PWOK asserted at turn on.	100	500	ms
T pwok_off	Delay from PWOK de-asserted to 12V output voltage dropping out of regulation limits.	1		ms
T psok_low	Duration of PWOK begin in the de-asserted state during an off/on cycle using DC input or the PSON# signal.	100		ms
T sb_vout	Delay from 12Vsb begin in regulation to O/Ps begin in regulation at DC input turn on.	10	1500	ms

Turn On/Off Timing (single Power supply)



4. CONTROL AND INDICATOR FUNCTIONS

The following section defines the input and output signals from the power supply.
Signals that can be defined as low true use the following convention:
Signal# = low true.

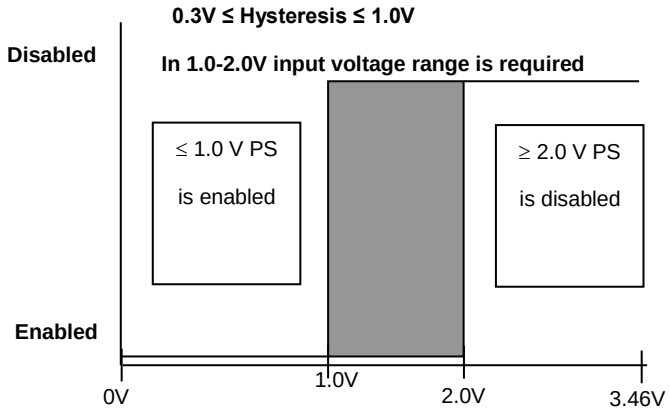
4.1 PSON# INPUT SIGNAL (POWER SUPPLY ENABLE)

The PSON# signal is required to remotely turn on/off the main output of the power supply. PSON# is an active low signal that turns on the main output power rail. When this signal is not pulled low by the system or left open, the outputs (except the Standby output) turn off. PSON# is pulled to a standby voltage by a pull-up resistor internal to the power supply.

PSON# Signal Characteristic

Signal Type	+3.3V TTL Compatible output signal	
PSON# = Low	ON	
PSON# = High or Open	OFF	
	MIN	**MAX**
Logic level low (power supply ON)	0V	1.0V
Logic level high (power supply OFF)	2.0V	3.46V
Source current, V_{pson} = low		4mA
Power up delay: $T_{pson\_on\_delay}$	5ms	400ms
PWOK delay: T_{pson_pwok}		50ms

PSON# Signal Characteristic



4.2 POWER OK (PWOK OR PG) BUS

PWOK is a power good signal and shall be pulled HIGH by the power supply to indicate that all outputs are within regulation limits. When any output voltage falls below regulation limits, an internal failure or when input power has been removed for a time sufficiently long, so that power supply operation is no longer guaranteed, PWOK will be de-asserted to a LOW state. The start of the PWOK delay time shall inhibited as long as any power supply output is in current limit.

PWOK / PG Signal Characteristics

Signal Type	+3.3V TTL Compatible output signal	
PWOK = High	Power OK	
PWOK = Low	Power Not OK	
	MIN	**MAX**
Logic level low voltage, I_{sink} = 4µA	0V	0.4V
Logic level high voltage, I_{source} = 200µA	2.4V	3.46V
Sink current, PWOK = low		400µA
Source current, PWOK = high		2mA
PWOK delay: T_{pwok_on}	100ms	500ms
PWOK rise and fall time		100µsec
Power down delay: T_{pwok_off}	1ms	200ms

4.3 SMBAlert# Signal

This signal indicates that the power supply is experiencing a problem that the user should investigate. This shall be asserted according to Critical or Warning events set in the SMBAlert_MASK. The SMBAlert_MASK default shall activate the signal in case of critical component and ambient temperature reached a warning threshold,Input UV failure , and over-current. This signal may also indicate the power supply is reaching its end of life or is operating in an environment exceeding the specified limits.

This signal is to be asserted in parallel with LED turning solid Amber or blink Amber.

SMBAlert# Signal Characteristics

Signal Type (Active Low)	Open collector / drain output from power supply. Pull-up to VSB located in system.	
Alert# = High	**OK**	
Alert# = Low	**Power Alert to system**	
	MIN	MAX
Logic level low voltage, Isink=4 mA	**0 V**	**0.4 V**
Logic level high voltage, Isink=50 µA		**3.46 V**
Sink current, Alert# = low		**4 mA**
Sink current, Alert# = high		**50 µA**
Alert# rise and fall time		**100 µs**

4.4 Cold Redundant-Bus# (CR_BUS) Signal [B22]

This signal is used for power supply to power supply communication in form of an interrupt. This interrupt is by default low impedance low. For all power supplies connected to this bus shall have an open collector and a pull high circuitry, which can provide at least 4mA.
This function shall be PMBus controlled and allows the system to set the power module into four different modes:

1. MASTER – Load dependent function
2. SLAVE – Load dependent function
3. MASTER – VDC Input dependent function
4. SLAVE – Master dependent function

SLAVE's in CR Standby shall provide PG and LED should be solid GREEN.

CR_BUS# Signal Characteristics

Signal Type (Active HIGH)	Open collector drain or Source output from power supply. Pull-up to VSB located in system.	
CR_BUS# = High	**CR Standby allowed**	
CR_BUS# = Low	**SLAVEs need to be Active on.**	
	MIN	MAX
Logic level low voltage, Isink=4 mA	**0 V**	**0.4 V**
Logic level high voltage, Isource=4 mA		**3.46 V**
Sink current, CR_BUS# = low		**4 mA**
Source current, CR_BUS# = high		**4 mA**
CR_BUS# rise and fall time		**100 μs**

4.5 Load sharing control (12V Load Share)

The +12 V output shall have active load sharing.

All current sharing functions shall be implemented internal to the power supply by making use of the 12VLS signal. The power distribution board (Housing or Back Plane), must connect the 12VLS signals between the power supplies together. The power supply shall be able to share with up to N+1 supply in parallel.

The failure of a power supply shall not affect the load sharing or output voltages of the other supplies still operating. The power supplies must be able to load share with 100mV of drop between different power supply's output.

If the load sharing is disabled by shorting the load share bus to ground, the power supply shall continue to operate within regulation limits for loads less than or equal to the rating of one power supply.

Load share bus output characteristics

Item	Description	Min	Nominal	Max	Units
V_{share}; I_{out}=Max.	Voltage of load share bus at specified max output current		8		V
$\Delta V_{share}/\Delta I_{out}$	Slope of load share bus voltage with changing load		0.175		V/A
I_{Share} Accuracy	Defines the tolerance between two units shall load share.	±0.5A		±5%	
T_{share}; I_{out}=Max.	Delay from output voltages in regulation to load sharing active with maximum load of one power supply and two power supplies in parallel. (remote on/off only)			100	msec

4.5.1 Hot Swap Requirements

Hot swapping a power supply is the process of inserting and extracting a power supply from an operating power system. During this process the output voltages shall remain within the limits with the capacitive load specified. The hot swap test must be conducted when the system is operating under static, dynamic and zero loading conditions. The power supply can be hot swapped by the following method:

Extraction: The power supply may be removed from the system while operating with PSON# asserted, while in standby mode with PSON# de-asserted or with no AC applied. No connector damage should occur during un-mating of the power supply from the power distribution board (PDB).

Insertion: The power supply may be inserted into the system with PSON# asserted, with PSON# de-asserted or with no AC power present for that supply. No connector damage should occur due to the mating of the output and input connector.

In general a failed (of by internal latch or external control) supply may be removed, then

replaced with a good power supply, however, hot swap needs to work with operational as well as failed power supplies. The newly inserted power supply will get turned on into standby or Power On mode once inserted.

The Power Supply shall meet following condition while hot swapping and operation:

1. Output voltages shall stay within regulations, in accordance of chapter 3.2.7.
2. Signal Outputs, as PWOK#, PSON#, SMB_ALERT#, SDA, SCL and other signals shall not oscillate or change.
3. Current share, compatibility, cold redundancy and PDB bus shall not oscillate
4. LED states shall not change
5. Inserted supplies shall always run synchronous in all operation stages. Any oscillation of voltage waveforms, due to non-synchronous operation is not acceptable.

4.6 PRESENT# Signal [B24]

This signal is used for system present identification. This Pin is tied to GND and shall sink any current to GND to signal the system that the power module had been asserted into the system.

4.7 REMOTE SENSE + / REMOTE SENSE -

These signals are analog In/Output 12V Main Voltage Sense. Both are analog input/output voltage sense lines to compensate for power path voltage drop. These low level analog signals should be isolated from digital circuit noise.

When one or more remote sense lines are opened, regulation measured at the power supply output connector must be maintained within regulation defined, plus or minus an additional 200mV.

If the REMOTE SENSE+ is shorted to DC_RETURN, the main 12V output shall go for protection and the power supply will shut down.

5. PROTECTION CIRCUITS

Protection circuits shall cause only the power supply's main outputs to shutdown (latch off). If the power supply latches off due to a protection circuit tripping, an DC cycle OFF for 15 second or a PSON# cycle HIGH for 1 second must be able to reset the power supply.

The auxiliary output shall not be affected by any protection circuit, unless the auxiliary output itself is affected.

5.1 CURRENT LIMIT

The power supply shall prevent the main and auxiliary outputs from exceeding the values shown in below Table. If the main current limits are exceeded the power supply will shut down and latch off, *the auxiliary output shall be auto recover* ***(Vsb_{AR})*** *after the OCP/SCP had been removed.*

Over Current Protection

Voltage	Over Current Limit (Iout limit)
+12V	110% minimum, 150% maximum
+12Vsb ***(Auxiliary)AR***	7.5A Maximum

5.2 OVER VOLTAGE PROTECTION

The power supply shall shutdown and latch off after an over voltage condition occurs. This latch will be cleared by toggling the PSON# signal or by a DC power interruption.
A shutdown caused by an over-voltage in one power supply will not cause the other (redundant) power supply to shuts down.
The over-voltage threshold is defined in table below.

Over Voltage Limits

Output Voltage	MIN (V)	MAX (V)
+12V	13.5	15
+12Vsb ***(Auxiliary)AR***	13.5	15

5.3 Output Under VOLTAGE PROTECTION

The power supply shall shutdown and latch off after the under voltage condition has occurred. This latch will be cleared by toggling the PSON# signal or by an Input power interruption.

A shutdown caused by an over-voltage in one power supply will not cause the other (redundant) power supply to shuts down.

The under-voltage threshold is defined in table below.

Under Voltage Limits

Output Voltage	MAX (V)
+12V	10.0

5.4 Input Protection$_{AR}$

The power supply shall be protected against Input failure conditions caused by loss of input source failures. In an input failure condition the power supply shall shutdown the main output at UVP or OVP, Standby will shutdown at UVP_{HW_OFF}, then recover after input power recover within regulation. The 12VSB shall not shutdown during an OVP or UVP condition on the main outputs.

The protection thresholds are listed in below table:

Input Type	UVP	UVP_{HW_OFF}	OVP
DC (-36Vdc ~ 72Vdc)	-32.5Vdc	-30Vdc	-80Vdc

5.5 OVER TEMPERATURE PROTECTION

The power supply shall be protected against over temperature conditions caused by loss of fan cooling or excessive ambient temperature which could cause internal part failures. In an over temperature condition the power supply shall shutdown, then recover after while the temperature back in normal condition. The 12VSB shall not shutdown during an OTP condition on the main outputs.

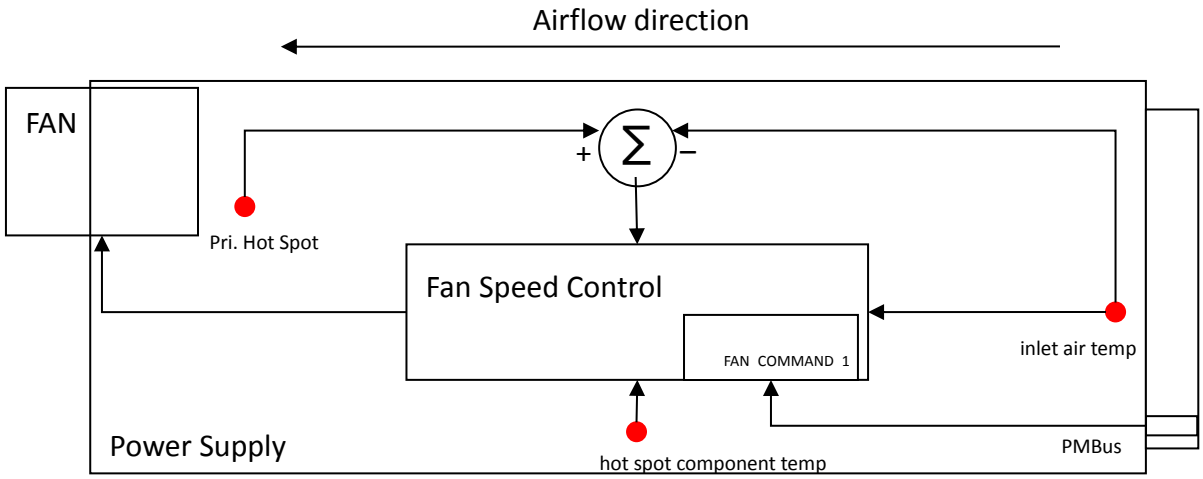
The temperature warning setting point is showing on below table:

Condition	Warning in °C	Critical in°C	Timing for SMBAlert#/LED
$T_{Ambient}$	58	68	100msec
$T_{Sec.\ Hot\ Spot}$	96	106	100msec
$T_{Pri.\ Hot\ Spot}$	90	100	100msec

5.6 Fan Control

The Power Supply shall a Fan speed control, which has a close loop algorithm based on the critical component temperature, the ambient temperature (Inlet temperature), primary side component temperature, and Output power. The fan speed control shall always increase the fan speed to protect the power supply in any airflow impedance condition and guarantee that the air flow is in proper direction through the power supply.

After Turn Off by PSON or Input Brown Out, the power supply will continue to control fan speed to reduce component temperatures within normal conditions, and turn off when acceptable component temperatures are meet. This function shall protect the power from over heating and reduced component life, due to instant airflow cut off.



6. LED IDENTIFICATION

There is one indicator LED located on the front faceplate.
There have five kinds of status showing on below:

Power Supply Condition	LED State
Output ON and OK	GREEN
No DC input power to all power supplies	OFF
DC input present / only 12Vsb on (PS off) or PS in Cold redundant state	1Hz Blink GREEN
DC input cord unplugged or DC input power lost; with a second power supply in parallel still with DC input power	AMBER
Power supply warning events where the power supply continues to operate high temp, high power, high current, slow FAN.	1Hz Blink AMBER
Power supply critical event causing a shutdown; failure, OCP, OVP, FAN fail.	AMBER

7. COLD REDUNDANCY SUPPORT

Power supplies that support cold redundancy can be enabled to go into a low-power state (that is, cold redundant state) in order to provide increased power usage efficiency when system loads are such that both power supplies are not needed. When the power subsystem is in Cold redundant mode, only the needed power supply to support the best power delivery efficiency is ON. Any additional power supplies; including the redundant power supply, is in Cold Standby state.
Each power supply has an additional signal that is dedicated to supporting *Cold Redundancy*; CR_BUS. This signal is a common bus between all power supplies in the system. CR_BUS is asserted when there is a fault in any power supply OR the power supplies output voltage falls below the V-fault threshold. Asserting the CR-BUS signal causes all power supplies in Cold Standby state to power ON.

Enabling power supplies to maintain best efficiency is achieved by looking at the Load Share bus voltage and comparing it to a programmed voltage level through a PMBus command.
Whenever there is no active power supply on the *Cold Redundancy* bus driving a HIGH level on the bus all power supplies are ON no matter their defined Cold Redundant roll (active or Cold Standby). This guarantees that incorrect programming of the *Cold Redundancy* states of the power supply will never cause the power subsystem to shut down or become over loaded. The default state of the power subsystem is all power supplies ON. There needs to be at least one power supply in *Cold Redundant* Active state or Standard Redundant state to allow the Cold Standby state power supplies to go into Cold Standby state.

7.1 COLD REDUNDANT

The power supply has Smart On redundant function. The Slave module shall be capable of being in the Cold Standby state when the system load is less than 40% of full load, and recovery to normal redundant state when the system is more than 70% of full load.

This Control is done by the CR Master and is not compatible with AC supply power modules.

AC power supply mixing would only allow Active-Standby mode, where the Slave is permenantly in Smart Standby state, indementent from load.

Smart Standby module will immediately turn on within 300uSec and output all of system power once the operating module predicts failure. The power supply module must meet the output regulation in section 2.3.2.

Command Code	Command Name	Read/ Write	Number of Data Bytes	Note
D0h	Cold Redundant Mode	R/W	1	0x00h: Normal Redundant Mode 0x01h: CR Main (Master) Mode Load 0x02h: CR Standby (Slave) Mode Load

7.1.1 *Power ON Initial Status*

Any Power Supply at start-up will be in default redundant mode.

7.1.2 *Normal Redundant Mode (00h)*

CR pin is set to low impedance low, assuring any accidental false setup.

This is default mode and be set via I_2C/PMBus command if value had been changed.

When power supply experience any fault this value will be set and system need to set CR-mode again in compliance with Intel requirements.

All active power supplies will active share current, when any power supply is set to this mode or a new power module is inserted into the power system.

7.1.3 *CR Master Load Mode (01h)*

Configured PSU in this mode, is allowed to drive CR pin high to inform any PSU set to slave PSU mode that it is allowed to go into CR-Standby mode, when condition are meet.

- **Set CR pin to low state** (all PSU shall provide output current, CR-Stb prohibited)

1. Any Fault or Output, Input out of regulation condition.
2. Output load is above 70% of full load, will also drive CR_Bus pin low, to wake any CR-Stb power module to provide best overall system efficiency.

- **Set CR pin to high state** (all PSU set as CR Slave can go to CR-Stb, depending on set mode)

In CR Master Load Mode, the CR_BUS pin will be driven high when Output load is below 40% of full load. This allows any CR Slave Load Mode to go into CR-Stb to save as much energy as possible, to allow the increase of the overall power system efficiency.

7.1.4 *CR Slave Load Mode (02h)*

CR pin will be set as input to read the CR_BUS pin level.

Any supply in this mode shall go and leave CR-Stb mode, depending on below CR_BUS pin condition.

- **CR pin is high**

CR Slave Load mode power supply is allowed to go into CR-Standby mode to save energy.

- **CR pin is low**

CR Slave Load mode power supply shall immediately power on or is not allowed to go into CR-Standby mode.

- **Slave Fault**

Any Slave experience any Fault (e.g. OC, OV, OT, OP, UV, Input, Fan) shall drive the CR_BUS pin low and preventing the power system to go into CR-Mode.

8. POWER SUPPLY MANAGEMENT

8.1 HARD WARE LAYER

The serial bus communication devices for Power Supply Management Controller (PSMC) and Field Replacement Unit (FRU) in the power supply shall be compatible with both SMBus 2.0 "high power" and I^2C Vdd based power and drive specification.

This bus shall operate at 3.3V but be tolerant to 5V pull-ups. The power supply should not have any internal pull-ups on the SMBus, pull-ups shall be located on system side.

Two pins are allocated on the power supply. One pin is the serial clock (SCL). The second pin is used for serial data (SDA). Both pins are bi-directional and are used to form a serial bus. The device(s) in the power supply shall be located at an address(s) determined by addressing pins A0 and A1 on the power supply module. The circuits inside the power supply shall derive their 3.3V power from the 12VSB bus through a buffer. Device(s) shall be powered from the system side of the 12VSB or'ing device. No pull-up resistors shall be on SCL or SDA inside the power supply. The pull-up resistors should be located external to the power supply on system/application side.

8.1.1 Capacitance for SMBus

The recommended Capacitance per pin on SDA and SCL shall be 10pF, and is not allowed to exceed 40pF per pin. In an N+1 configuration of up to four (4) power modules with additional PDB, the total Capacitance of each Bus pin shall not exceed 400pF.

8.1.2 I^2C Bus Noise Requirement

The power supplies I^2C Bus' SDA and SCL line shall be clean from noise, which might affect the proper function when utilized with other devices.

The maximum allowed line noise on SDA or SCL is 300mV .

8.2 POWER SUPPLY MANAGEMENT CONTROLLER *(PSMC)*

The PSMC device on the PDB shall derive its power of the 12Vsb output on the system side of the O'ring device and shall be grounded to return. It shall be compatible with SMBus specification 2.0 and PMBus™ Power System Management Protocol Specification Part I and Part II in Revision 1.2 or later

It shall be located at the address set by the A0 and A1 pins.

Refer to the specification posted on www.ssiforum.org and www.pmbus.org website for details on the power supply monitoring interface requirements and refer to followed section of supported features. The below table reflect the power module addresses complying with the position in the housing.

PDB position and PSMC address	**PM1 B0h/B1h**	**PM2 B2h/B3h**	**PM3 B4h/B5h**	**PM4 B6h/B7h**
Pin A0/A1	0/0	1/0	0/1	1/1

8.2.1 Power Supply Field Replacement Unit (FRU)

The power supply shall support electronic access of FRU information over an I^2C bus. Six pins at the power supply connector are allocated for this. They are named SCL, SDA, A2, A1, A0 and Write protect. SCL is serial clock. SDA is serial data. These two bidirectional signals from the basic communication lines over the I^2C bus. A0, A1 and A2 are input address lines to the power supply. The backplane defines the state of these lines such that the address to the power supply is unique within the system. The resulting I^2C address shall be per table below. The Write protection pin is to ensure that data will not accidentally overwritten.

The device used for this shall be powered from a 3.3V bias voltage derived from the +12 VSB output . No pull-up resistors shall be on SCL or SDA inside the power supply.

PDB position and FRU address	PM1 A0h/A1h	PM2 A2h/A3h	PM3 A4h/A5h	PM4 A6h/A7h
Pin A1/A0	0/0	0/1	1/0	1/1

8.3 Sensor Accuracy

The sensor of the PSMC shall meet below accuracy requirements for sensor readings. The accuracy shall be met at the specified environmental condition and the full range of rated input voltage.

Sensor Accuracy Table

Sensor	10% - 20% load	> 20% - 50% load	> 50% - 100% Load
Output Current	± 5% or 0.5A	± 5%	± 5%
Input Current	± 5% or 0.5A	± 5%	± 5%
Voltage	± 5%	± 5%	± 5%
Temperature	± 5 °C		
Input Power	± 5% or 10W	± 5%	± 5%
Output Power	± 5% or 5W	± 5%	± 5%

***** PMBus compliance please refer to firmware specification *****

9. ENVIRONMENTAL

9.1 TEMPERATURE REQUIREMENTS

The power supply shall operate within all specified limits over the Top temperature range. The average air temperature difference ($\triangle T_{ps}$) from the inlet to the outlet of the power supply shall not exceed the values shown below Table. All airflow shall pass through the power supply and not over the exterior surfaces of the power supply

ITEM	DESCRIPTION	MIN	MAX	UNITS
T_{op}	Operating temperature range.	0	50	°C
$T_{non\text{-}op}$	Non-operating temperature range.	-40	70	°C

9.2 HUMIDITY

Operating: 5% to 95% relative humidity, non-condensing.
Storage: 5% to 95% relative humidity, non-condensing.

9.3 ALTITUDE

Operating: 5,000m

9.4 VIBRATION

Operating: 0.01G2/Hz at 10Hz, 0.02G2/Hz at 20Hz.
Non-Operating: 0.02G2/Hz form 20Hz to 1000Hz.

9.5 MECHANICAL SHOCK

Operating: 5G, no malfunction.
Non-operating: 50G, no damage. Trapezoidal Wave, Velocity change = 4.3m/sec. Three drops in each of six directions are applied to each of the samples.

9.6 EMI/EMC REQUIREMENTS

The power supply shall comply the radiated emissions of Class A requirement in GR-1089-CORE, Issue 6 section 3.2.1 and conducted emissions requirement in section 3.2.2.

The power supply shall comply meet FCC part 15, CRISP 22 and EN55022.
Class A for both conducted and radiated emissions with a 6dB margin.

The test shall be conducted using a shielded DC output cable to a shielded load. The load shall be adjusted to 100% load. Tests will be performed full load on each output power at -48VDC.
The test set-up and measurement technique shall be in accordance with the following test procedure standards:
EN 61000-4-3: 2008 Testing and measurement techniques—Radiated, radio-frequency, electromagnetic field immunity test, 3V/m, 80MHz to 1GHz
EN 61000-4-4: 2004 (Electrical Fast Transient/Burst). (1K)
EN 61000-4-6: 2008 (Conducted RF immunity 3V/m, 0.15MHz to 80MHz)
EN 61000-4-8:2009 (Power Frequency Magnetic Field) including A1:2001.

10.REGULATORY REQUIREMENTS

10.1 PRODUCT SAFETY COMPLIANCE

The power supply will have the following safety approvals with most current editions:

A) UL 60950-1/CSA 60950-1 Edition 2 (USA/Canada)
B) TUV EN60950-1 Edition 2 (Europe)
C) IEC60950-1 Edition 2 (International)
D) CB Certificate & Report, IEC60950-1 Edition 2
E) CE – Low Voltage Directive 2006/95/EC (Europe)
F) KCC (Korea)
G) CCC / GB17625-2012 Certification (China)

10.2 ELECTROSTATIC DISCHARGE

The objective of ESD test is to determine the susceptibility and immunity of products to electrostatic discharge to which the products may be exposed, when operating under all potential environmental conditions. The test conditions and setup shall conform to that outlined in CISPR24-2 and IEC 801-2 (EN55101-2).
Air discharge: 8KV not allow error.
Contact discharge: 4KV not allow error.
Note: The above test discharge time is 1 time/sec and repeats each test 10 times.

10.3 HI-POT

All production unit must pass a 1414Vdc Hi-Pot test between primary to chassis ground or follow safety agency, with a trigger limit of 500uA.

11.RELIABILITY

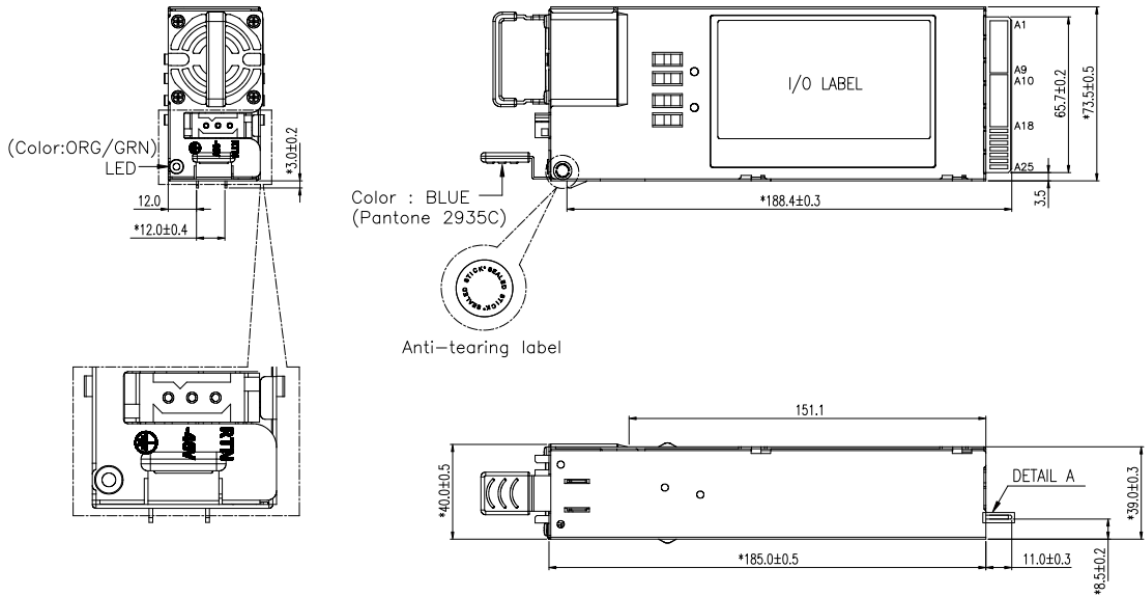
The MTBF of the power supply can be calculated with the Part-Stress Analysis method of Bell Core SR332 of the quality factors. A calculated MTBF of the power supply shall be at least 100,000 hours at 25°C ambient with -48VDC and in full load condition.

12. RoHS COMPLIANCE

The directive 2002/95/EC of the European Parliament and of the Council of the 27th January 2003, on the restriction of the use of certain hazardous substances in electrical and electronic equipment, requires the reduction of the substances Lead, Mercury, Cadmium, Hexavalent Chromium, Polybrominated Biphenyls (PBB), and Polybrominated Biphenyl ethers (PBDE) in electronic products by July 1, 2006. Unless otherwise noted, all materials used will be compliant with this directive and any subsequent revisions or amendments.

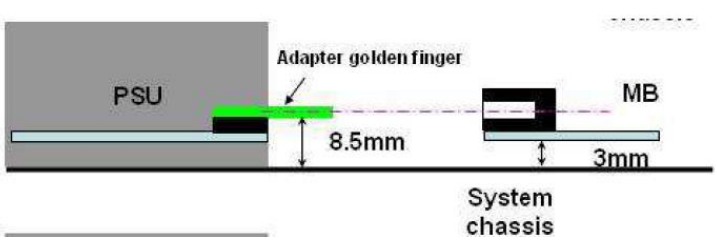
13. MECHANICAL DIMENSIONS

Dimension (L x W x H): 185 x 73.5 x 40mm / 7.28 x 2.89 x 1.57inch

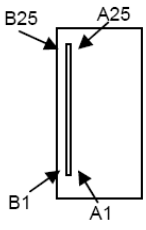


NOTE: Above drawing is for reference only, detail dimension should refer to independent mechanical drawing.

The height of adapter gold finger to the bottom is 8.5mm

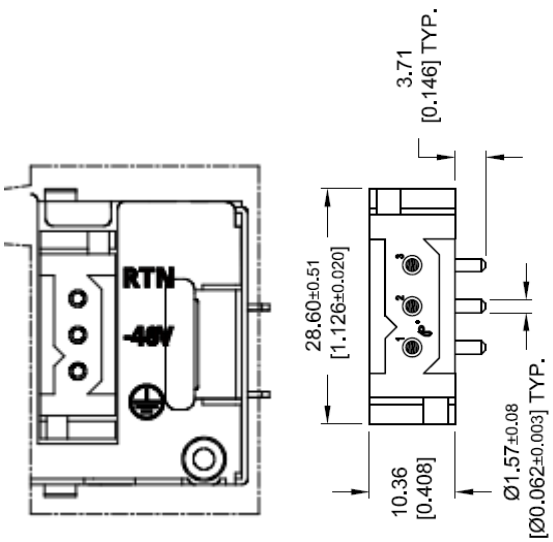


FCI 2x25 card edge connector 10035388-102



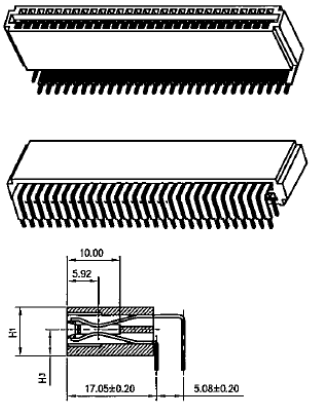
13.1 DC Input connector

The power supply shall use a DC input connector for input power connection. The connector should use equivalent to ***POSITRONIC PN# PLAH03M400A1/AA-E1A.***



13.2 DC Output connector

The power supply shall use a card edge output connection for power and signal that is compatible with a 2x25 Power Card Edge connector (equivalent to 2x25 pin configuration of the FCI power card connector 10035388-102LF or ALLTOP C21009-102H3-Y).



Gold finger pin assignment

OUTPUT PIN ASSIGNMENT

PIN	SIGNAL_NAME	PIN	SIGNAL_NAME
A1	GND	B1	GND
A2	GND	B2	GND
A3	GND	B3	GND
A4	GND	B4	GND
A5	GND	B5	GND
A6	GND	B6	GND
A7	GND	B7	GND
A8	GND	B8	GND
A9	GND	B9	GND
A10	+12V	B10	+12V
A11	+12V	B11	+12V
A12	+12V	B12	+12V
A13	+12V	B13	+12V
A14	+12V	B14	+12V
A15	+12V	B15	+12V
A16	+12V	B16	+12V
A17	+12V	B17	+12V
A18	+12V	B18	+12V
A19	PMBus SDA	B19	A0 (SMBus address)
A20	PMBus SCL	B20	A1 (SMBus address)
A21	PSON	B21	12VSB
A22	SMBAlert#	B22	CR_BUS#
A23	Return Sense	B23	12V load share Bus
A24	+12V Remote Sense	B24	PRESENT#
A25	PWOK	B25	NC

14. Supported Command Summary

Command Code (Hex)	Command Name	Transaction Type	Number of Data Bytes
00h	PAGE	W/R Byte	1
01h	OPERATION	W/R Byte	1
02h	ON_OFF_CONFIG	W/R Byte	1
03h	CLEAR_FAULTS	Send Byte	0
05h	PAGE_PLUS_WRITE	Block WRITE	Variable
06h	PAGE_PLUS_READ	Block READ	Variable
0Ch	MFR_HEALTH_READ	Read Byte	1
10h	WRITE_PROTECT	W/R Byte	1
19h	CAPABILITY	Read Byte	1
1Ah	QUERY	BW/BR Process Call	1
1Bh	SMBALERT_MASK	Write W & BW/BR PC	2
20h	VOUT_MODE	Read Byte	1
30h	COEFFICIENTS	BW/BR Process Call	5
31h	POUT_MAX	Read Word	2
3Ah	FAN_CONFIG_1_2	W/R Byte	1
3Bh	FAN_COMMAND_1	W/R WORD	2
40h	VOUT_OV_FAULT_LIMIT	Read Word	2
42h	VOUT_OV_WARN_LIMIT	W/R Word	2
43h	VOUT_UV_WARN_LIMIT	W/R Word	2
44h	VOUT_UV_FAULT_LIMIT	Read Word	2
46h	IOUT_OC_FAULT_LIMIT	Read Word	2
4Ah	IOUT_OC_WARN_LIMIT	W/R Word	2
4Fh	OT_FAULT_LIMIT	Read Word	2
51h	OT_WARN_LIMIT	W/R Word	2
55h	VIN_OV_FAULT_LIMIT	Read Word	2
57h	VIN_OV_WARN_LIMIT	W/R Word	2
58h	VIN_UV_WARN_LIMIT	W/R Word	2
59h	VIN_UV_FAULT_LIMIT	Read Word	2
68h	POUT_OP_FAULT_LIMIT	Read Word	2
6Ah	POUT_OP_WARN_LIMIT	W/R Word	2
6Bh	PIN_OP_WARN_LIMIT	W/R Word	2
78h	STATUS_BYTE	W/R Byte	1
79h	STATUS_WORD	W/R Word	2
7Ah	STATUS_VOUT	W/R Byte	1

Command Code (Hex)	Command Name	Transaction Type	Number of Data Bytes
7Bh	STATUS_IOUT	W/R Byte	1
7Ch	STATUS_INPUT	W/R Byte	1
7Dh	STATUS_TEMPERATURE	W/R Byte	1
7Eh	STATUS_CML	W/R Byte	1
7Fh	STATUS_OTHER	W/R Byte	1
80h	STATUS_MFR_SPECIFIC	W/R Byte	1
81h	STATUS_FAN_1_2	W/R Byte	1
86h	READ_EIN	Block READ	5
87h	READ_EOUT	Block READ	5
88h	READ_VIN	Read WORD	2
89h	READ_IIN	Read WORD	2
8Bh	READ_VOUT	Read WORD	2
8Ch	READ_IOUT	Read WORD	2
8Dh	READ_TEMP_ENV	Read WORD	2
8Eh	READ_TEMP_HS_SEC	Read WORD	2
8Fh	READ_TEMP_HS_PRI	Read WORD	2
90h	READ_FAN_SPEED_1	Read WORD	2
96h	READ_POUT	Read WORD	2
97h	READ_PIN	Read WORD	2
98h	PMBUS_REVISION	Read BYTE	1
99h	MFR_ID	BW/BR	5 (Acbel)
9Ah	MFR_MODEL	BW/BR	14 (R1CD2xxxx-P000)
9Bh	MFR_REVISION	BW/BR	3 (A00)
9Ch	MFR_LOCATION	BW/BR	3 (PRC or TWN)
9Dh	MFR_DATE	BW/BR	6 Integer (YYMMDD)
9Eh	**MFR_SERIAL**	**BW/BR**	**25**
9Fh	APP_PROFILE_SUPPORT	Rlock READ	Variable
A0h	MFR_VIN_MIN	Read Word	2
A1h	MFR_VIN_MAX	Read Word	2
A2h	MFR_IIN_MAX	Read Word	2
A3h	MFR_PIN_MAX	Read Word	2
A4h	MFR_VOUT_MIN	Read Word	2
A5h	MFR_VOUT_MAX	Read Word	2
A6h	MFR_IOUT_MAX	Read Word	2
A7h	MFR_POUT_MAX	Read Word	2

Command Code (Hex)	Command Name	Transaction Type	Number of Data Bytes
A8h	MFR_TAMBIENT_MAX	Read Word	2
A9h	MFR_TAMBIENT_MIN	Read Word	2
AAh	MFR_EFFICIENCY_LL	Block READ	14
ABh	MFR_EFFICIENCY_HL	Block READ	14
C0h	MFR_MAX_TEMP_ENV	Read Word	2
C1h	MFR_MAX_TEMP_HS1	Read Word	2
C2h	MFR_MAX_TEMP_HS2	Read Word	2
D0h	MFR_COLD_REDUNDANT_CONFIG	W/R Byte	1
D9h	***MFR_FW_REVISION***	***Block Read***	***4 (0000)***
FEh	MFR_SPECIFIC_COMMAD_EXT	Extended Command	MFR Defined
FFh	PMBUS_COMMAND_EXT	Extended Command	MFR Defined

15. FRU SEEPROM (IPMI)

The Power Supply shall have a FRU device in compliance with IPMI specification Rev. 1.1 from November 15th 1999.

FRU Content is as follow.

	0x0	0x1	0x2	0x3	0x4	0x5	0x6	0x7	0x8	0x9	0xA	0xB	0xC	0xD	0xE	0xF
0x00	01	00	00	00	01	0B	00	F3	01	0A	19	C5	41	43	42	45
0x01	4C	CB	52	31	43	44	32	35	35	31	41	20	20	C6	46	53
0x02	45	30	33	39	C4	41	32	41	47	D8	46	53	45	30	33	39
0x03	41	30	30	41	32	41	47	42	31	35	35	30	30	30	30	30
0x04	30	31	C3	41	30	30	CA	41	50	4D	31	33	56	30	30	30
0x05	34	C1	00	00	00	00	00	37	00	02	18	8A	5C	26	02	CB
0x06	02	28	0A	10	E	20	1C	0	0	0	0	00	00	0A	1F	CB
0x07	F2	00	00	00	0F	01	02	0D	AF	41	01	B0	04	8C	04	D4
0x08	04	78	00	00	00	09	B3	01	82	0D	27	49	82	B0	04	8C
0x09	04	D4	04	78	00	00	00	B8	0B	FF	FF	FF	FF	FF	FF	FF
0xA0	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
0xB0	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
0xC0	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
0xD0	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
0xE0	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
0xF0	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF

= Checksum

= Area Start

= Asset Tag MFG REV

= Product mfg product name

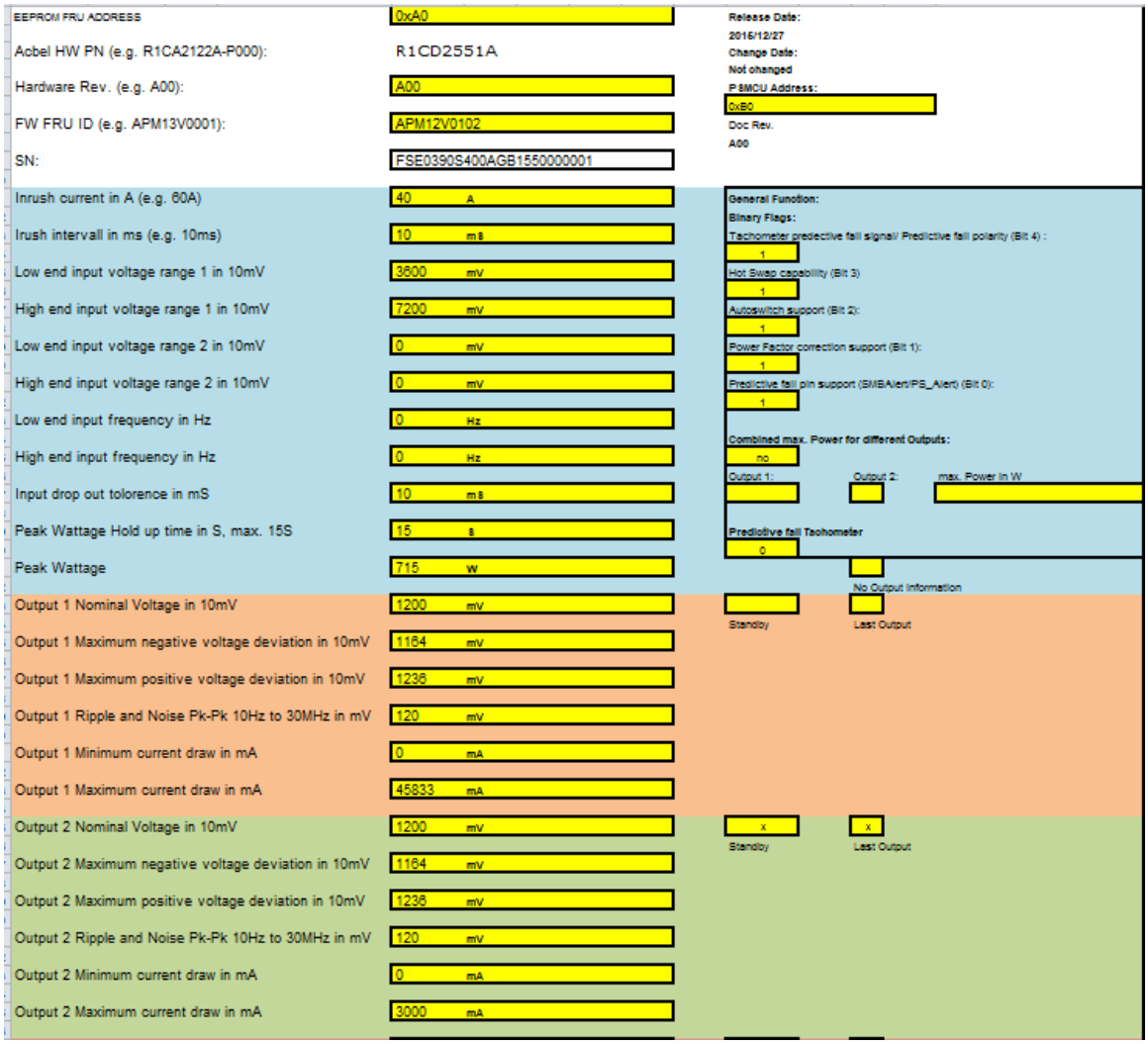
= Product mfg SN

= Product mfg PN & Rev.

= Product mfg FRU ID

= C1h Indicator for no more info fields

= Empty



EEPROM FRU ADDRESS	0xA0	Release Date: 2016/12/27
Acbel HW PN (e.g. R1CA2122A-P000):	R1CD2551A	Change Date: Not changed
Hardware Rev. (e.g. A00):	A00	P.8MCU Address: 0xB0
FW FRU ID (e.g. APM13V0001):	APM12V0102	Doc Rev. A00
SN:	FSE0390S400AGB1550000001	
Inrush current in A (e.g. 60A)	40 A	General Funotion:
Irush intervall in ms (e.g. 10ms)	10 mS	Binary Flags: Tachometer predective fall signal/ Predictive fall polarity (Bit 4) : 1
Low end input voltage range 1 in 10mV	3600 mV	Hot Swap capability (Bit 3) 1
High end input voltage range 1 in 10mV	7200 mV	Autoswitch support (Bit 2): 1
Low end input voltage range 2 in 10mV	0 mV	Power Factor correction support (Bit 1): 1
High end input voltage range 2 in 10mV	0 mV	Predictive fall pin support (SMBAlert/PS_Alert) (Bit 0): 1
Low end input frequency in Hz	0 Hz	Combined max. Power for different Outputs:
High end input frequency in Hz	0 Hz	no
Input drop out tolorence in mS	10 mS	Output 1: Output 2: max. Power in W
Peak Wattage Hold up time in S, max. 15S	15 S	Predicitve fall Tachometer 0
Peak Wattage	715 W	No Output Information
Output 1 Nominal Voltage in 10mV	1200 mV	Standby Last Output
Output 1 Maximum negative voltage deviation in 10mV	1164 mV	
Output 1 Maximum positive voltage deviation in 10mV	1236 mV	
Output 1 Ripple and Noise Pk-Pk 10Hz to 30MHz in mV	120 mV	
Output 1 Minimum current draw in mA	0 mA	
Output 1 Maximum current draw in mA	45833 mA	
Output 2 Nominal Voltage in 10mV	1200 mV	x x Standby Last Output
Output 2 Maximum negative voltage deviation in 10mV	1164 mV	
Output 2 Maximum positive voltage deviation in 10mV	1236 mV	
Output 2 Ripple and Noise Pk-Pk 10Hz to 30MHz in mV	120 mV	
Output 2 Minimum current draw in mA	0 mA	
Output 2 Maximum current draw in mA	3000 mA	